

SERIAL EEPROM 512K/1M
PN 2280007900G for 1Mbit (PM25LV010A-100SCE)

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Date: Thursday, May 21, 2009
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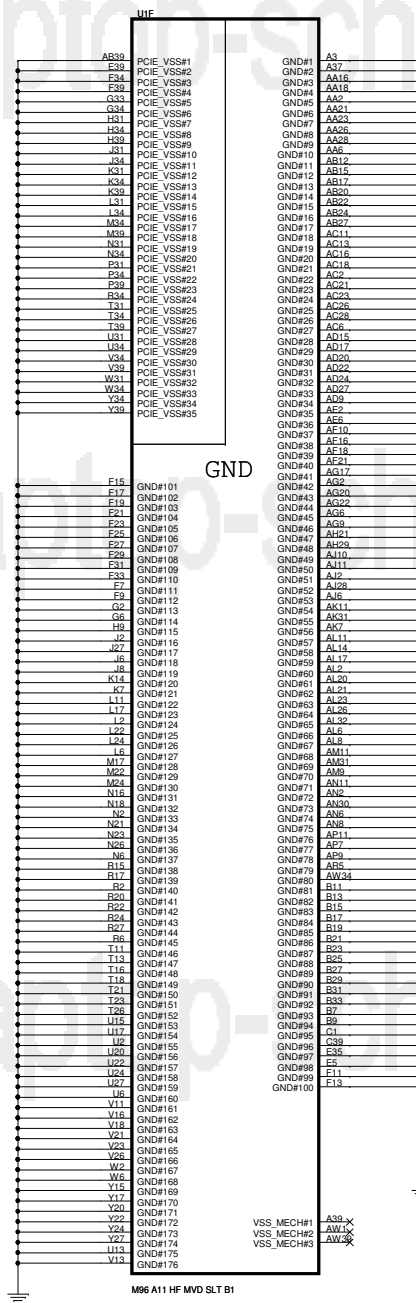
Rev 3

Doc No. 105-B803xx-00D

AMD

Pin RH M96 GDDR3 MxM3.0





M96 A11 HF MVD SLT B1

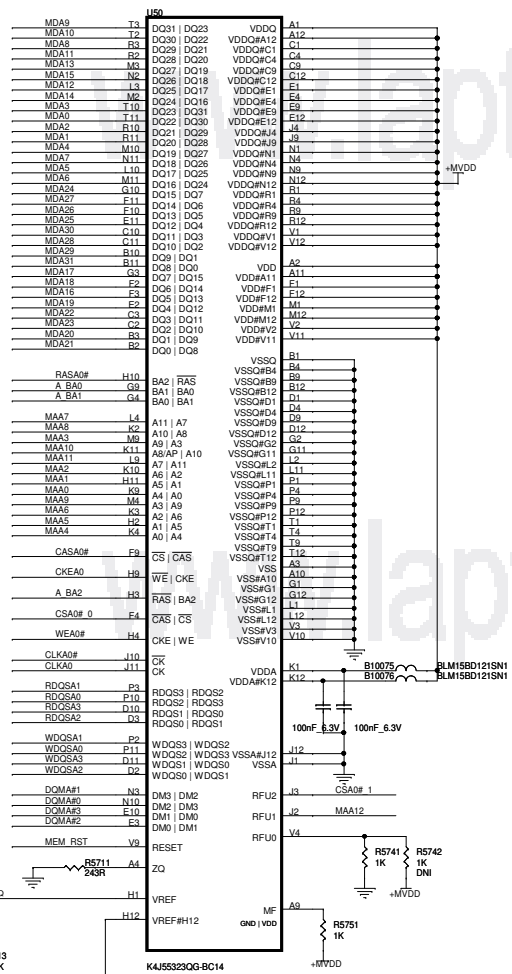
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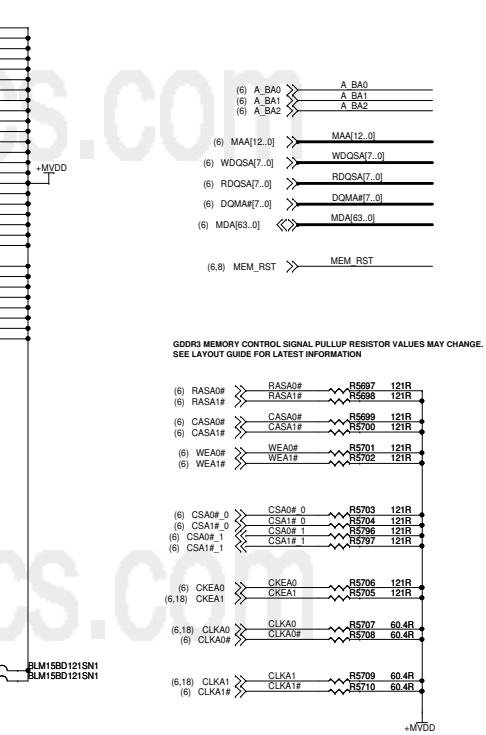
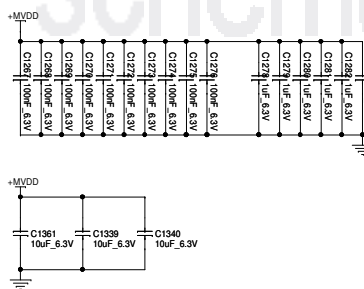
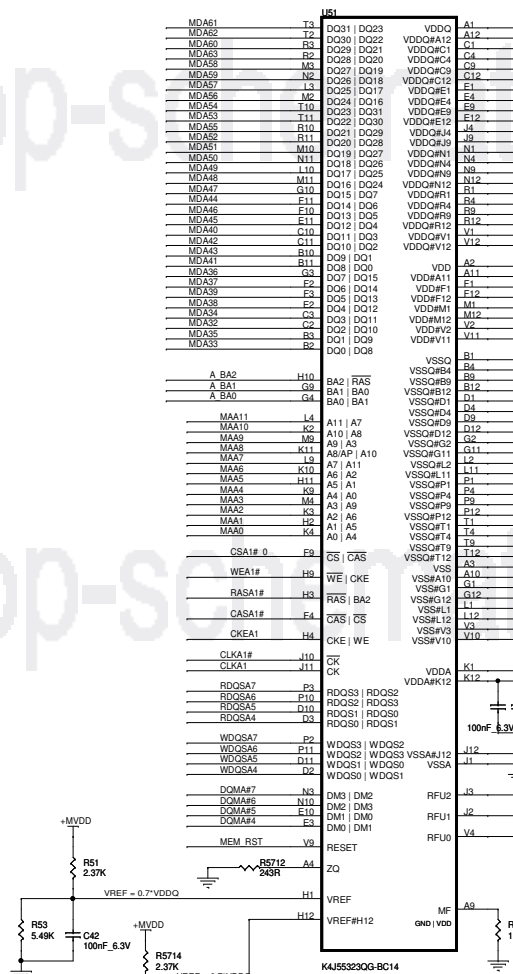
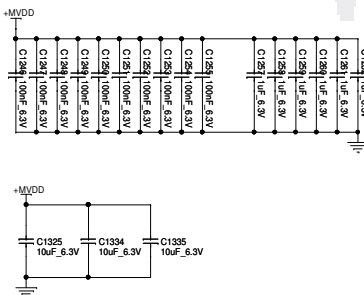
File: RH M96 GDDP3 MxM3.0



GDDR3 32X32 MEMORY



PLACE VREF DIVIDER COMPONENTS
AS CLOSE TO MEMORY AS POSSIBLE



**GDDR3 MEMORY CONTROL SIGNAL PULLUP RESISTOR VALUES MAY CHANGE.
SEE LAYOUT GUIDE FOR LATEST INFORMATION**

(6)	RASAD#	RASAD#	R5697	121R
(6)	RASA1#	RASA1#	R5698	121R
(6)	CASAD#	CASAD#	R5699	121R
(6)	CASA1#	CASA1#	R5700	121R
(6)	WEAD#	WEAD#	R5701	121R
(6)	WEA1#	WEA1#	R5702	121R
(6)	CSAD#_0	CSAD#_0	R5703	121R
(6)	CSA1#_0	CSA1#_0	R5704	121R
(6)	CSAD#_1	CSAD#_1	R5705	121R
(6)	CSA1#_1	CSA1#_1	R5707	121R
(6)	CKEAD#	CKEAD#	R5706	121R
(6,18)	CKEA1	CKEA1	R5705	121R
(6,18)	CLKAD#	CLKA0	R5707	60.4R
(6,18)	CLKA0#	CLKA0#	R5708	60.4R
(6,18)	CLKA1	CLKA1	R5709	60.4R
(6,18)	CLKA1#	CLKA1#	R5710	60.4R

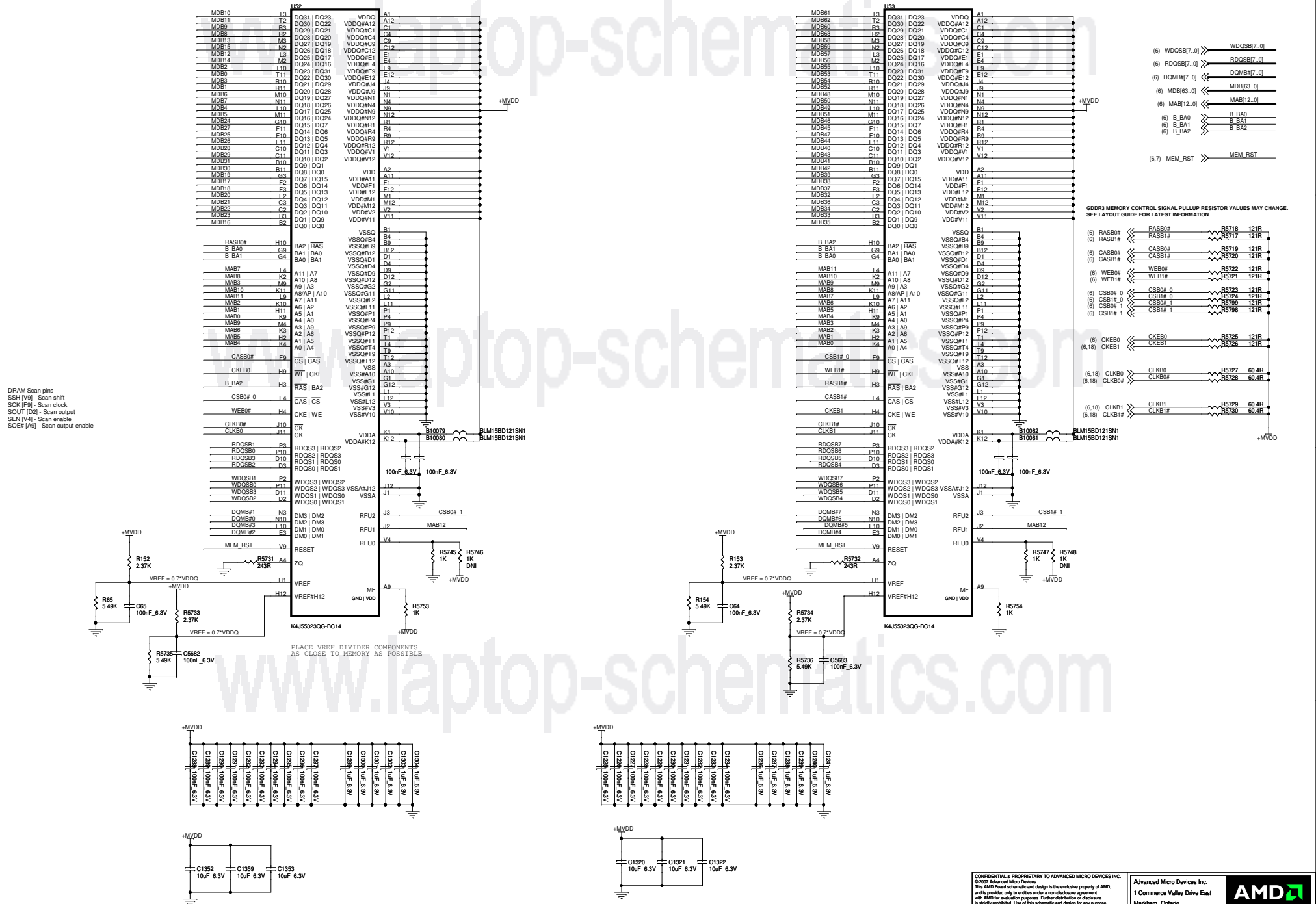
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
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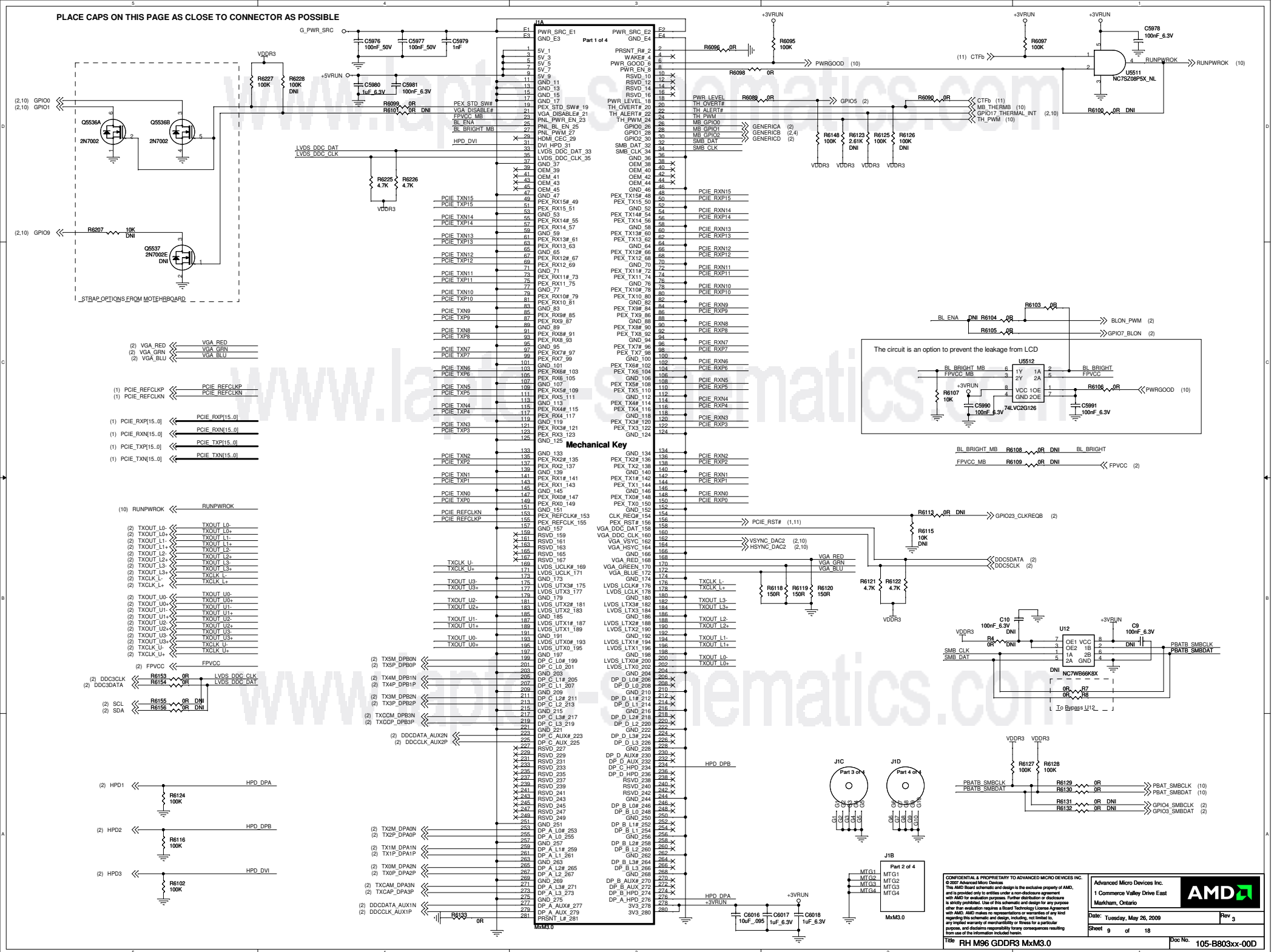
GDDR3 32X32 MEMORY

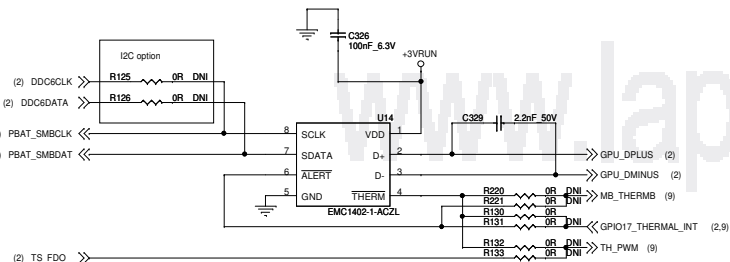
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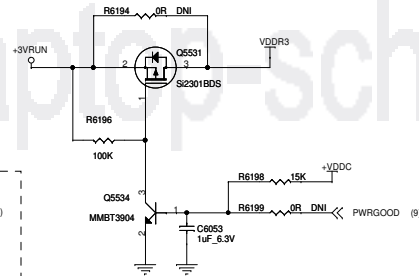
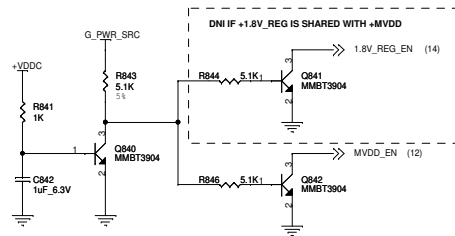
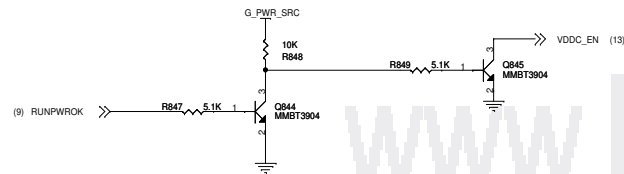
Title	RH M96 GDDR3 MxM3.0
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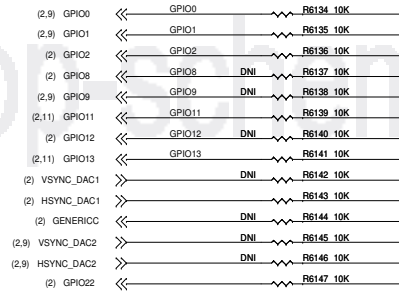


Power Up Sequence



VDDR3 Enable Circuit

PIN STRAPS

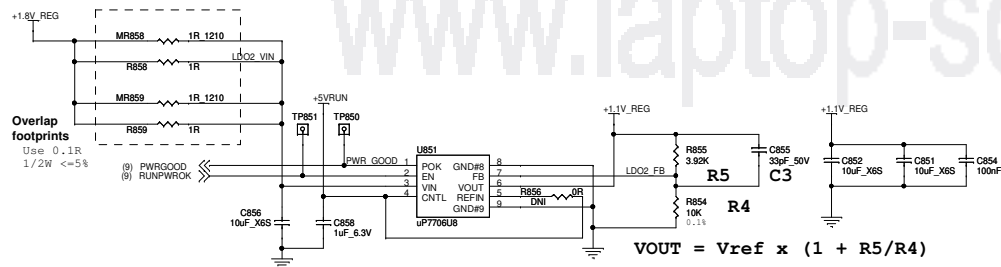


CONFIGURATION STRAPS

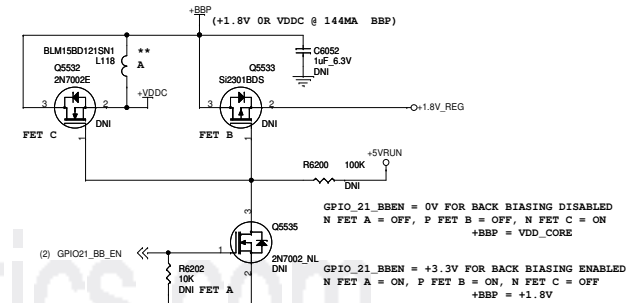
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	0
TX_DEEMPH_EN	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	0
BIF_GEN2_EN_A	GPIO2	PCIe Gen2 Enable 0: Advertises the PCIe device as 2.5GT/s capable at power-on 1: Advertises the PCIe device as 5.0GT/s capable at power-on	1
BIF_CLK_PM_EN	GPIO8	Master control for CLKREQb 0: Disabled 1: Enabled	0
BIF_VGA_DIS	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	1
ROMIDCF[2:0]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type	100 - 512Kb M25P16A (ST) 101 - 1Mb M25P16A (ST) 101 - 2Mb M25P16A (ST) 101 - 4Mb M25P16A (ST) 101 - 8Mb M25P16A (ST) 100 - 512Kb M25P16A (ST) 101 - 1Mb M25P16A (ST) 101 - 2Mb M25P16A (ST)
VIP_DEVICE_STRAP_ENA	V2SYN	VIP Device Strap Enable 0: Slave VIP host port devices present 1: No slave VIP host port devices reporting presence	0
AUD[1] AUD[0]	HSYN VSYN	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
SMS_EN_HARD CCBYPASS	HSYN GENERICC	Reserved	N/A

LDO #2: Vin = +1.8V +/-5% Vout = +1.1V +/- 2% Iout = 1.7A (TBV) RMS MAX
PCB: 50 to 70mm sq. copper area for cooling



$$VOUT = Vref \times (1 + R5/R4)$$



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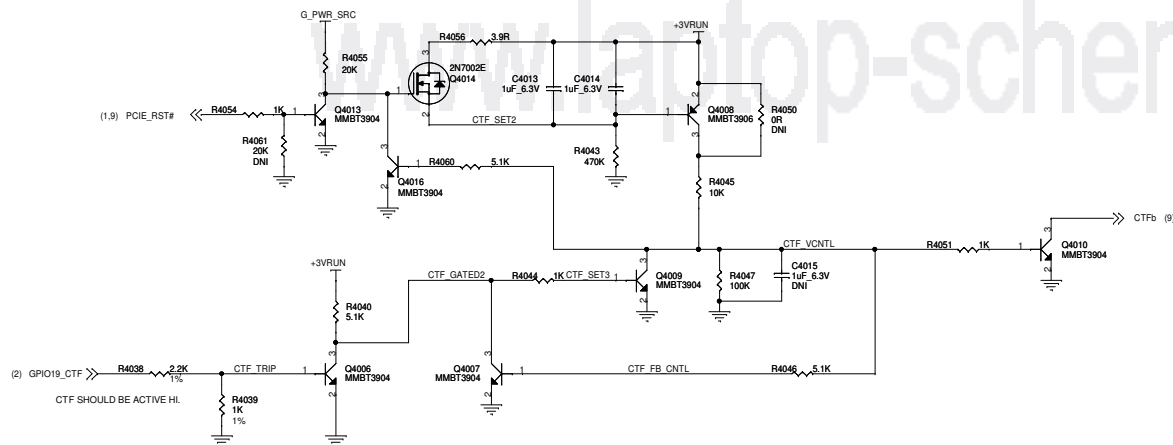
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Part RH M96 GDDR3 MxM3.0

Critical Temperature Fault



Power Play

GPIO20	GPIO15	VDDC
0	0	1.20V
0	1	1.12V
1	0	1.04V
1	1	0.95V

(2,10) GPIO13
(2,10) GPIO15
(2) GPIO20

VID for VDDC Setting

For GPIO11 and GPIO13, see straps table.

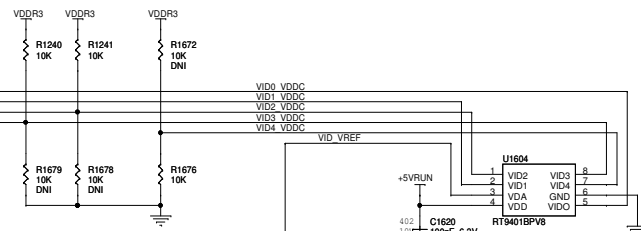
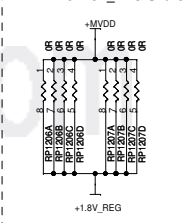


Table 4 VDDC Vref Mode Selection

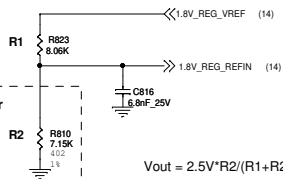
Vref Mode	R636	R639/C659	Vref (V)
Internal	Populate	NC	0.6
External	NC	Populate	set by VID IC (U1604)

MVDD & 1.8V_REG Share



DNI IF +1.8V_REG IS SHARED WITH +MVDD

For Version 2 1.8V_REG Controller

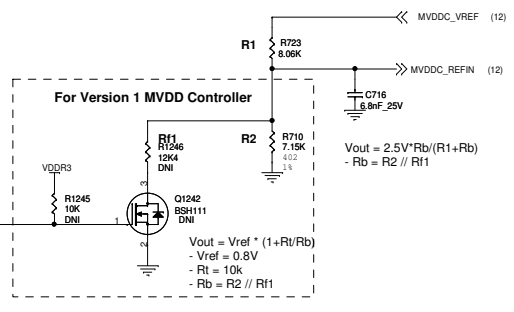


For Version 1 1.8V_REG Controller

$$V_{out} = V_{ref} * (1 + R1/R2)$$

- Vref = 0.8V
- Rt = 10k

For Version 2 MVDD Controller



For Version 1 MVDD Controller

GPIO6	MVDD
0	TBD
1	TBD

(2) GPIO6

$$V_{out} = V_{ref} * (1 + R1/Rb)$$

- Vref = 0.8V
- Rt = 10k
- Rb = R2 // Rt

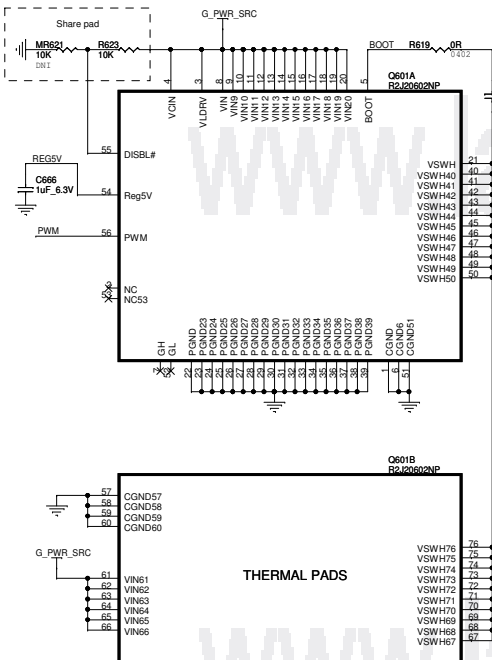
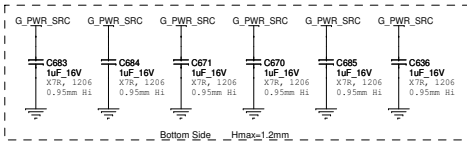
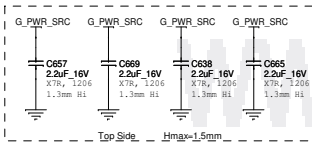
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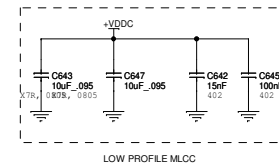
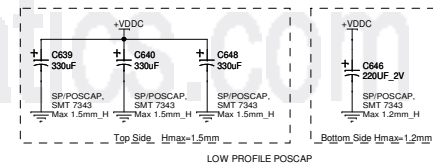
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Title: RH M96 GDDR3 MxM3.0

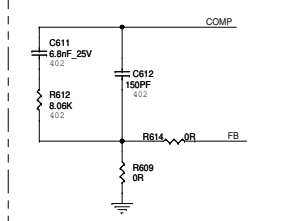
INPUT CAP



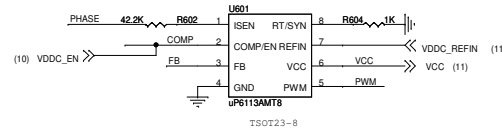
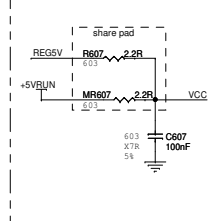
OUTPUT CAP




COMPENSATION CIRCUIT



FILTERED SMPS VCC



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Title: RH M96 GDDR3 MxM3.0

Top Side

Four capacitors are shown, each connected to a +5VRLN rail and ground:

- C721**: 2.2uF, 16V, X7R, 1206, 1.3mm HI
- C732**: 2.2uF, 16V, X7R, 1206, 1.3mm HI
- C726**: 2.2uF, 16V, X7R, 1206, 1.3mm HI
- C727**: 2.2uF, 16V, X7R, 1206, 1.3mm HI

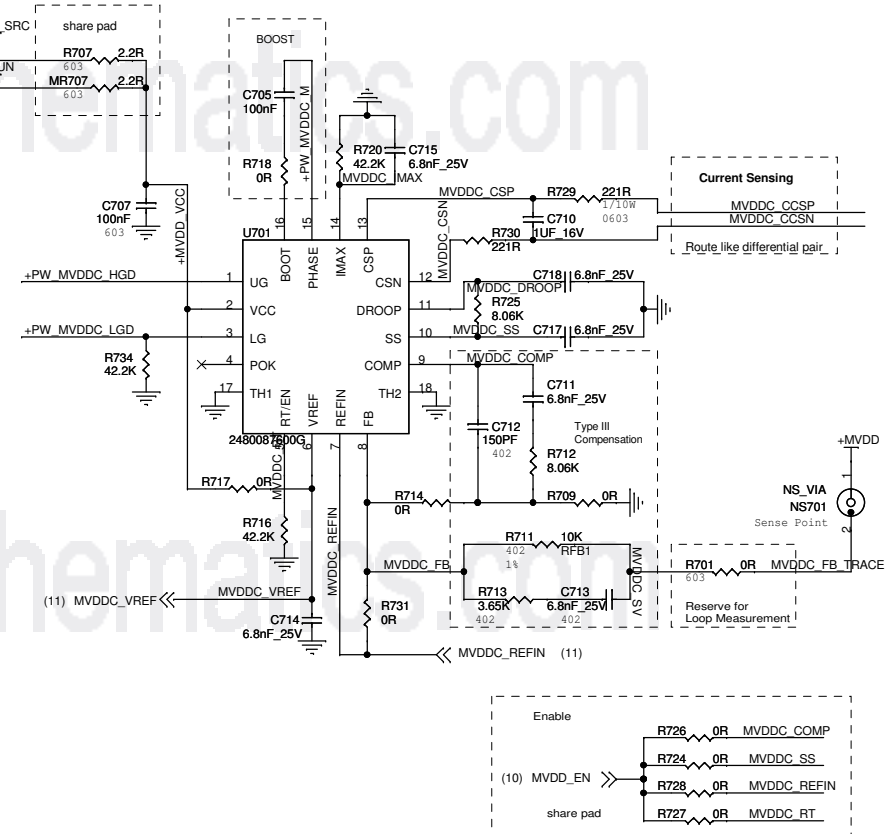
Dimensions: $H_{max} = 1.5mm$

Bottom Side

Two capacitors are shown, each connected to a +5VRLN rail and ground:

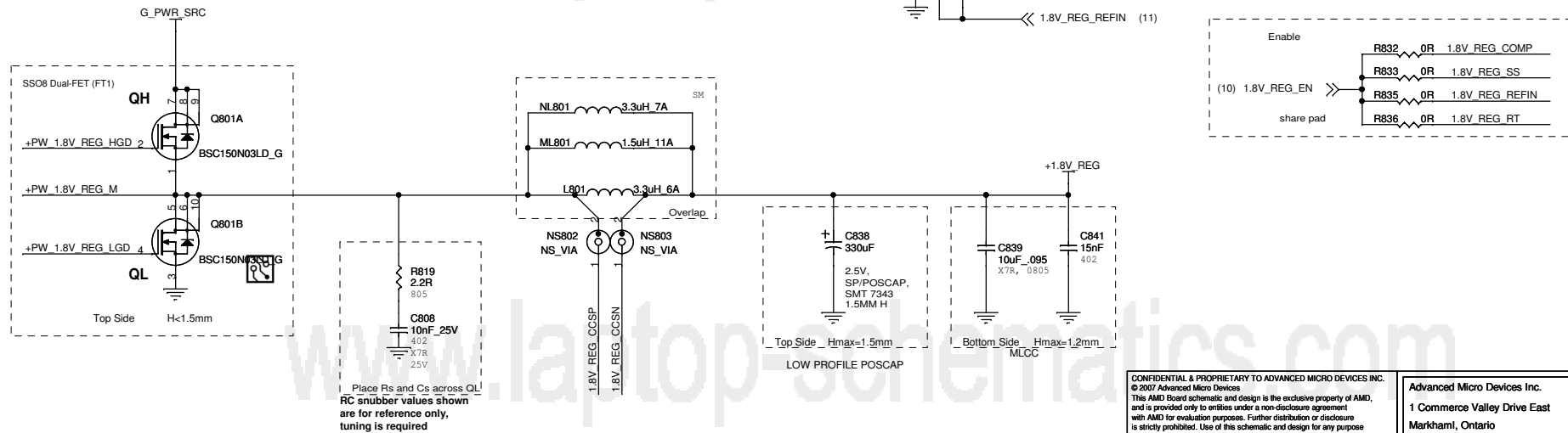
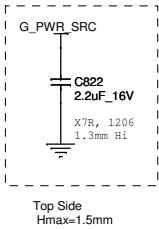
- C730**: 1uF, 16V, X7R, 1206, 0.95mm HI
- C733**: 1uF, 16V, X7R, 1206, 0.95mm HI

Dimensions: $H_{max} = 1.2mm$



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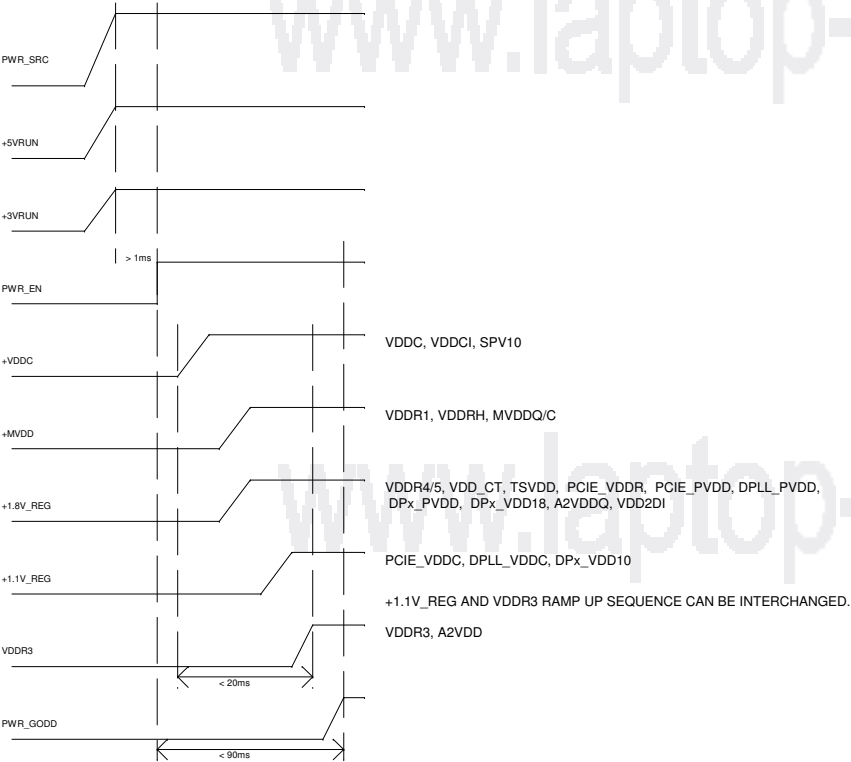
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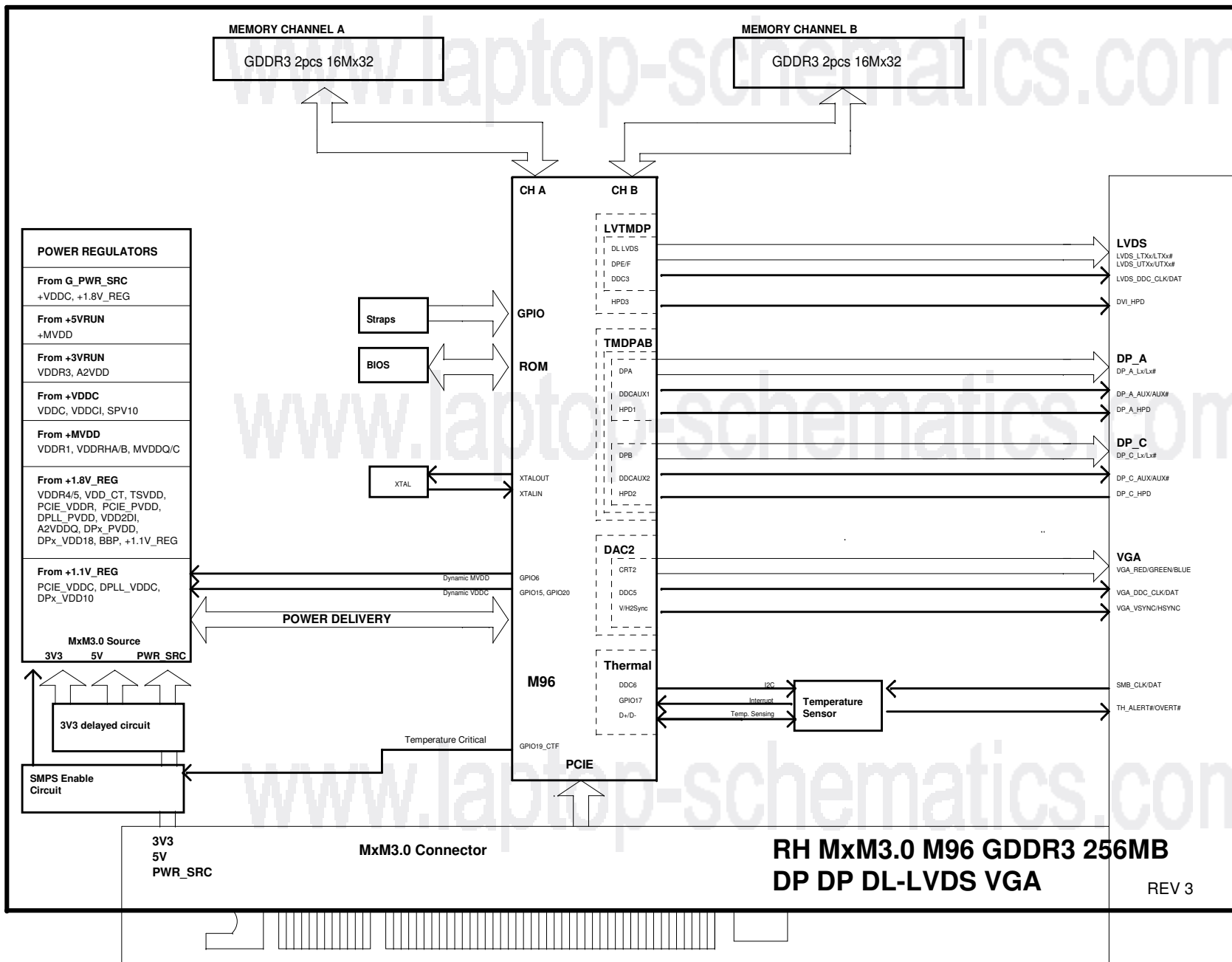
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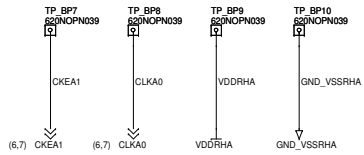
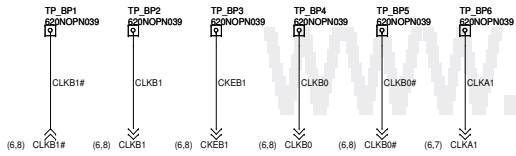
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POWER UP SEQUENCE (not to scale)






<div>AMD</div>			Title		Schematic No.		Date:	
			RH M96 GDDR3 MxM3.0		105-B803xx-00D		Thursday, May 21, 2009	
			REVISION HISTORY		NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI's, ...) please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.			
Sch Rev	PCB Rev	Date	REVISION DESCRIPTION					
0	00A	08/12/31	Initial design for M96 GDDR3 MxM3.0 based on B703-00C					
1	00B	09/04/15	Add boundry scan feature for DRAMs; Add R5751~R5754 Add R5741~R5748 Add a series resistor (R1000) and a shunt cap (C1000) to mem_rst					
2	00C	09/04/22	Add R6227, R6228 Update J1 (non-plated holes connected to ground)					



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